This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended) A charge pump circuit comprising:

a first native transistor with a threshold voltage that is greater than zero over a voltage range caused by process variations;

first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage, wherein the first native transistor and the first depletion transistors are coupled together in series between an input and an output of the charge pump circuit; and

first capacitors, wherein a drain of each of the first depletion transistors is coupled to one of the first capacitors, a first subset of the first capacitors are coupled to receive a first clock signal, and a second subset of the first capacitors are coupled to receive a second clock signal.

Claim 2 (currently amended) ~~The charge pump circuit of claim 1 further comprising:~~

A charge pump circuit comprising:

a first native transistor;

first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage, wherein the first native transistor and the first depletion transistors are coupled together in series between an input and an output of the charge pump circuit;

first capacitors, wherein a drain of each of the first depletion transistors is coupled to one of the first capacitors, a first subset of the first capacitors are coupled to receive a first clock signal, and a second subset of the first capacitors are coupled to receive a second clock signal; and

second depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first depletion transistors at a common source voltage,

wherein a drain of each of the second depletion transistors is coupled to one of the first capacitors, and

the first native transistor, the first depletion transistors, and the second depletion transistors are all coupled together in series between the input and the output of the charge pump circuit.

Claim 3 (previously presented) The charge pump circuit of claim 2 wherein the first depletion transistors include at least four depletion transistors, and the second depletion transistors include at least four depletion transistors.

Claim 4 (previously presented) The charge pump circuit of claim 3 wherein the first depletion transistors include at least six depletion transistors, and the second depletion transistors include at least six depletion transistors.

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Claim 5 (currently amended) The charge pump circuit of claim ~~1~~ 2 further comprising diode-connected transistors, wherein each diode-connection transistor is coupled to a gate of one of the first depletion transistors.

Claim 6 (previously presented) The charge pump circuit of claim 4 wherein the first depletion transistors include at least seven depletion transistors, and the second depletion transistors include at least seven depletion transistors.

Claim 7 (currently amended) The charge pump circuit of claim ~~1~~ 2 further comprising:

a second native transistor that is coupled in series with the first native transistor.

Claim 8 (previously presented) The charge pump circuit of claim 2 wherein each of the first depletion transistors have a negative threshold voltage implant region with a first concentration of an N-type dopant, and each of the second depletion transistors have a negative threshold implant region with a second concentration of the N-type dopant, the second

concentration of the N-type dopant being greater than the first concentration of the N-type dopant.

Claim 9 (previously presented) The charge pump circuit of claim 2 further comprising:

second capacitors, wherein a gate of each of the first and the second depletion transistors and the first native transistor is coupled to one of the second capacitors, a first subset of the second capacitors are coupled to receive a third clock signal, and a second subset of the second capacitors are coupled to receive a fourth clock signal.

Claim 10 (currently amended) ~~The charge pump circuit of claim 1 further comprising:~~

A charge pump circuit comprising:

a first native transistor;

first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage, wherein the first native transistor and the first depletion transistors are coupled together in series between an input and an output of the charge pump circuit;

first capacitors, wherein a drain of each of the first depletion transistors is coupled to one of the first capacitors, a first subset of the first capacitors are coupled to receive a first clock signal, and a second subset of the first capacitors are coupled to receive a second clock signal; and

a second native transistor coupled to a gate, a drain, and a source of the first native transistor; and

third native transistors, wherein a gate, the drain, and a source of each of the first depletion transistors are coupled to one of the third native transistors.

Claim 11 (canceled)

Claim 12 (currently amended) A method for receiving an input voltage and providing a boosted output voltage, the method comprising:

boosting the input voltage by applying a first clock signal to a drain of a first native transistor, the first native transistor having a threshold voltage that remains greater than zero despite process variations; and

boosting a source voltage of the first native transistor by applying the first clock signal and a second clock signal to a drain and a source of each of a first set of depletion transistors that are coupled together in series to provide an output voltage,

the first set of depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage.

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Claim 13 (currently amended) ~~The method of claim 12 further comprising:~~

A method for receiving an input voltage and providing a boosted output voltage, the method comprising:

boosting the input voltage by applying a first clock signal to a drain of a first native transistor; and

boosting a source voltage of the first native transistor by applying the first clock signal and a second clock signal to a drain and a source of each of a first set of depletion transistors that are coupled together in series to provide an output voltage,

the first set of depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage; and

boosting the output voltage of the first native transistors by applying the first clock signal and the second clock signal to a drain and a source of each of a second set of depletion transistors that are coupled together in series and to the first depletion transistors,

the second set of depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first set of depletion transistors at a common source voltage.

Claim 14 (previously presented) The method of claim 13 wherein the gate of each of the first and the second sets of depletion transistors and the first native transistor is coupled to receive a third clock signal or a fourth clock signal.

Claim 15 (previously presented) The method of claim 14 wherein the first set of depletion transistors includes at least four depletion transistors, and the second set of depletion transistors includes at least four depletion transistors.

Claim 16 (previously presented) The method of claim 15 wherein the first set of depletion transistors includes at least six depletion transistors, and the second set of depletion transistors includes at least six depletion transistors.

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Claim 17 (currently amended) The method of claim 16 wherein the first set of depletion transistors includes at least seven depletion transistors, and the second ~~sert~~ set of depletion transistors includes at least seven depletion transistors.

Claim 18 (previously presented) The method of claim 14 wherein each of the first set of depletion transistors has a negative threshold voltage implant region with a first concentration of dopant, and each of the second set of depletion transistors has a negative threshold implant region with a second concentration of dopant, the second concentration of dopant being greater than the first concentration of dopant.

Claim 19 (previously presented) The method of claim 13 wherein:

a second native transistor is coupled to a gate, a drain, and source of the first native transistor; and

third native transistors that are each coupled to a gate, the drain, and the source of one of the first and the second sets of depletion transistors.

Claim 20 (canceled)

Claim 21 (previously presented) A charge pump circuit comprising:

a first native transistor;

first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage;

second depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first depletion transistors at a common source voltage, wherein the first native transistor, the first depletion transistors, and the second depletion transistors are all coupled in series between an input and an output of the charge pump circuit;

first capacitors that are each coupled to a first clock signal and to the first and the second depletion transistors; and

second capacitors that are each coupled to a second clock signal and to the first and the second depletion transistors.

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Claim 22 (previously presented) The charge pump circuit of claim 21 wherein the first and second clock signals are HIGH concurrently for a fraction of a clock period.

Claim 23 (previously presented) The charge pump circuit of claim 22 further comprising:

third and fourth capacitors that are coupled to gates of alternating ones of the first and the second depletion transistors.

Claim 24 (previously presented) The charge pump circuit of claim 23 wherein the third capacitors are coupled to receive a third clock signal, the fourth capacitors are coupled to receive a fourth clock signal, and the third and the fourth clock signals having non-overlapping HIGH pulses.

Claim 25 (previously presented) The charge pump circuit of claim 21 wherein the first depletion transistors include at least four depletion transistors, and the second depletion transistors include at least four depletion transistors.

Claim 26 (previously presented) The charge pump circuit of claim 21 wherein the first depletion transistors include at least six depletion transistors, and the second depletion transistors include at least six depletion transistors.

Claim 27. (previously presented) The charge pump circuit of claim 21 further comprising:

a second native transistor that is coupled in series with the first native transistor.

Claim 28 (previously presented) The charge pump circuit of claim 21 further comprising:

a second native transistor coupled to a gate, a drain, and source of the first native transistor; and

third native transistors that are each coupled to a gate, a drain, and a source of one of the first and the second depletion transistors.

Claim 29 (canceled)